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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,855	07/22/2003	Koichi Sato	Q76641	6425

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SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, DC 20037-3213

EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,855	SATO ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,8-12,14,18-22,24 and 28-30* is/are rejected.

7)☒ Claim(s) *3,5-7,13,15-17,23 and 25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/623,855 filed 07/22/2003.

2. Claims 1-30 are pending in the Application.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the element "CUP interface" mentioned in the claims 2, 12, 22 and in the Specification (pages 4, 7 and 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 2-7, 12-17 and 22-27 are objected to because of the following informalities: Applicant must identify what the acronym "CUP" (claims 2, 12 and 22) stands for, which is not clear from Specification (pages 4, 7 and 10).

Claim 3 line 3 after "and" delete "sad" insert –the--

Claim 13 line 2 after "and" delete "sad" insert –the--

Claim 23 line 3 after "and" delete "sad" insert –the--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 4, 8-12, 14, 18-22, 24, 28-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikegami (US Patent 6,782,354).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claims 1, 11 and 21 Ikegami teaches a circuit designing method, a circuit designing system, a computer program product within a method of producing simulation models (col. 2, ll.44-45) during the automatic designing process of the large-scaled circuits (col. 1, ll.12-14) including a simulation system (col. 18, l.39) and computer program product as a recording medium (col. 20, ll.63-65) comprising: (a) separating a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generating a design data automatically, wherein the design data includes behavior data, architecture data, mapping data and address data within the simulation system shown on the Fig. 2 wherein an algorithm level verifying section 1 is composed of an algorithm system 2 is divided into algorithm description model 3 as hardware (H/W) model and C language program 4 as software (S/W) model (col. 5, ll.63-67), wherein the design contained in the hardware and so9ftware is analyzed and verified by verification tools and the data is: functions of designed semiconductor device (col. 18, ll.4-7), architecture of the modules under verifying process (col. 8, ll.52-53), addresses, terminals and mapping (col. 9, ll.3-5); (b) generating a first clock base description automatically based on the design data, wherein the first clock base description describes relation between the hardware portion and the software portion within describing a semiconductor device to be simulated (designed) in the C language program (S/W) and the processing by the

hardware (H/W) is described in the algorithm description model 3 as shown on the Fig. 2 (col. 6, ll.1-4) and as a result the algorithm system 2 is converted into an algorithm level simulation model (first clock base description) outputted automatically as an algorithm level simulator 5 as shown on the Fig. 2 (col. 6, ll.5-9; col. ll.23-29); (c) generating a second clock base description automatically based on the design data, wherein the second clock base description describes the hardware portion within the clock level system 7 shown on the Fig. 2, which is composed of a clock level simulation (SIM) model 8 automatically processed through model converting tool 13 having a tool of the behavior synthesis tool 12 (col. 6, ll.15-18), wherein SIM model 8 (second clock base description) contain only information of hardware portion since only data from algorithm description 3 (H/W) was inputted into the process of generating SIM model 8 (second clock base description) as shown on the Fig. 2; and (d) generating a first CPU model automatically based on the design data, wherein the first CPU model describes the software portion, wherein the first clock base description, the second clock base description and the first CPU model are used for verifying the design data within generating CPU model 9 shown on the Fig. 2, wherein the clock level CPU model 9 automatically produced from C language program 4 (S/W portion) by C language compiler 11 (col. 6, ll.14-16), wherein algorithm simulator 5 (first clock base description), SIM model 8 (second clock base description) and CPU model 9 are components of the clock level verifying section 6 of the clock level system 7 as shown on the Fig. 2 (col. 6, ll.11-11).

With respect to claims 9, 19 and 29 Ikegami teaches a circuit designing method, a circuit designing system, a computer program product within a method of producing simulation models (col. 2, ll.44-45) during the automatic designing process of the large-scaled circuits (col. 1, ll.12-14) including a simulation system (col. 18, l.39) and computer program product as a recording medium (col. 20, ll.63-65), comprising: (h) separating a first algorithm description for a simulation into a hardware portion describing hardware and a software portion describing software, and generating a design data automatically, wherein the design data includes behavior data, architecture data, mapping data and address data within the simulation system shown on the Fig. 2 wherein an algorithm level verifying section 1 is composed of an algorithm system 2 is divided into algorithm description model 3 as hardware (H/W) model and C language program 4 as software (S/W) model (col. 5, ll.63-67) wherein the design contained in the hardware and so9ftware is analyzed and verified by verification tools and the data is: functions of designed semiconductor device (col. 18, ll.4-7), architecture of the modules under verifying process (col. 8, ll.52-53), addresses, terminals and mapping (col. 9, ll.3-5); (i) generating a first clock base description automatically based on the design data, wherein the first clock base description describes relation between the hardware portion and the software portion within describing a semiconductor device to be simulated (designed) in the C language program (S/W) and the processing by the hardware (H/W) is described in the algorithm description model 3 as shown on the Fig. 2 (col. 6, ll.1-4) and as a result the algorithm system 2 is converted into an algorithm level simulation model (first clock base description) outputted automatically as an algorithm level

simulator 5 as shown on the Fig. 2 (col. 6, ll.5-9; col. ll.23-29); (j) generating a second clock base description automatically based on the design data, wherein the second clock base description describes the hardware portion within the clock level system 7 shown on the Fig. 2, which is composed of a clock level simulation (SIM) model 8 automatically processed through model converting tool 13 having a tool of the behavior synthesis tool 12 (col. 6, ll.15-18), wherein SIM model 8 (second clock base description) contain only information of hardware portion since only data from algorithm description 3 (H/W) was inputted into the process of generating SIM model 8 (second clock base description) as shown on the Fig. 2; (k) generating a first CPU model automatically based on the design data, wherein the first CPU model describes the software portion within generating CPU model 9 shown on the Fig. 2, wherein the clock level CPU model 9 automatically produced from C language program 4 (S/W portion) by C language compiler 11 (col. 6, ll.14-16); and (l) carrying out the simulation to verify the design data by using the first clock base description, the second clock base description and the first CPU model within algorithm simulator 5 (first clock base description), SIM model 8 (second clock base description) and CPU model 9, which are components of the clock level verifying section 6 of the clock level system 7 as shown on the Fig. 2 (col. 6, ll.11-11; col. 8, ll.32-33, ll.46-48; col. 9, ll.15-19) using the ability of mixed simulation technique including switching between a plurality of simulation models (col. 1, ll.61-65).

With respect to claims 2-8 Ikegami teaches:

Claims 2, 12, and 22: step (b) includes: (b 1) generating an address decoder portion automatically in the first clock base description based on the address data as

shown on the Fig. 5 which represents an example of the an algorithm description model 3 shown on the Fig. 2 including datapath between registers and their addresses (col. 9, ll.38-41), wherein the address decoder portion describes an address decoder which is arranged between a bus and a CUP interface in the first clock base description and selects an algorithm block from a plurality of algorithm blocks as shown on the Fig. 4 depicting the process of defining elements of the designed semiconductor device, such as registers and memories and generating the datapath which is arranged between bus simulation model and GUI controller 41;

Claims 4, 14 and 24: step (a) includes: (a1) converting the first algorithm description into second algorithm description automatically within a description conversion by a model conversion tool 13 obtaining the data from the behavioral synthesis tool 12 (algorithm description) as shown on the Fig. 2 (col. 6, ll.16-18), wherein it is easier for the second algorithm description to be separated into the hardware portion and the software portion than for the first algorithm description by obtaining the output from the model conversion tool 13 (second algorithm description) as shown on the Fig. 2 and separating it into clock level SIM model 8 (hardware portion) and CPU model 9 (software portion) (col. 6, ll.);

Claims 8, 10, 18, 20, 28 and 30 : further comprising: (e) generating a first HDL description automatically based on the design data, wherein the first HDL description indicates relation between the hardware portion and the software portion within describing a semiconductor device to be simulated (designed) in the C language program (S/W) and the processing by the hardware (H/W) is described in the algorithm

description model 3 as shown on the Fig. 2 (col. 6, ll.1-4) and as a result the algorithm system 2 is converted into an algorithm level simulation model (first clock base description) outputted automatically as an algorithm level simulator 5 as shown on the Fig. 2 (col. 6, ll.5-9; col. ll.23-29); (f) generating a second HDL description automatically based on the design data, wherein the second HDL description indicates the hardware portion within obtaining RTL HDL 17 from behavior synthesis tool 12 as shown on the Fig. 2 (col. 6, ll.28-30); and (g) generating a second CPU model automatically based on the design data within obtaining CPU model 18 (Fig. 2) (col. 6, ll.25-28), wherein the second CPU model indicates the software portion, wherein the first HDL description, the second HDL description and the second CPU model are used for verifying the design data (col. 6, ll.22-24).

Allowable Subject Matter

7. Claims 3, 5-7, 13, 15-17, 23 and 25-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach generating a bus connection between the bus and the the address decoder which is described by using a virtual bus in the first clock base description; detecting first algorithm blocks from a plurality of algorithm blocks included in the first algorithm, wherein data flow in one way between the first algorithm blocks through a global variable and replacing the global variable associated with the first algorithm blocks to a port as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800